WHAT IS CLAIMED IS:

1. A method for forming a semiconductor device, comprising:

forming a fin structure;

forming a source region at one end of the fin structure;

forming a drain region at an opposite end of the fin structure;

forming an insulating layer in the fin structure, source region, and drain region, the insulating layer separating the fin structure into a first fin structure and second fin structure, the source region into a first source region and a second source region, and the drain region into a first drain region and a second drain region, the first fin structure, the first source region, and the first drain region being formed on an opposite side of the insulating layer of the second fin structure, the second source region, and the second drain region;

forming a gate dielectric layer on surfaces of the first and second fin structures, the first and second source regions, the first and second drain regions, and the insulating layer;

removing portions of the gate dielectric layer to create covered portions and bare portions;

depositing a gate material over the covered portions and bare portions;

doping the first fin structure, the first source region, and the first drain region with a first material;

doping the second fin structure, the second source region, and the second drain region with a second material; and

selectively removing portions of the gate material to form the semiconductor device.

2. The method of claim 1 wherein the forming an insulating layer includes:

forming the insulating layer to a width ranging from about 20 Å to about 30 Å.

3. The method of claim 1 wherein the forming a gate dielectric layer includes:

forming the gate dielectric layer to a thickness ranging from about 10 Å to about 30 Å.

4. The method of claim 1 wherein the depositing a gate material includes:

depositing the gate material to a thickness ranging from about 200 Å to about 1000 Å.

5. The method of claim 1 wherein a width of the covered portions of the gate dielectric layer ranges from about 100 Å to about 1000 Å.

6. The method of claim 1 wherein the first fin structure, first source region, and the first drain region are part of an N-channel device, and

wherein the second fin structure, the second source region, and the second drain region are part of a P-channel device.

7. The method of claim 1 wherein the selectively removing portions of the gate material includes:

removing a portion of the gate material located above the insulating layer in the source region of the semiconductor device.

8. The method 7 wherein a width of the portion of gate material ranges from about 100 Å to about 1000 Å.

9. The method of claim 1 wherein the semiconductor device includes an inverter.

10. The method of claim 1 wherein the semiconductor device includes a NAND gate.

11. The method of claim 1 wherein the semiconductor device includes a NOR gate.

12. A method for forming a semiconductor device from a device that includes a first source region, a first drain region, and a first fin structure that are separated from a second source region, a second drain region, and a second fin structure by an insulating layer, the method comprising:

forming an oxide layer over the device;

removing portions of the oxide layer to create alternating covered portions and bare portions;

depositing a gate material over the alternating covered portions and bare portions;

doping the first fin structure, the first source region, and the first drain region with a first material;

doping the second fin structure, the second source region, and the second drain region with a second material; and

removing a portion of the gate material above the insulating layer and over at least one covered portion to form the semiconductor device.

13. The method of claim 12 wherein the forming an oxide layer includes:

forming the oxide layer to a thickness ranging from about 100 Å to about 500 Å.

14. The method of claim 12 wherein a width of at least one covered portion ranges from about 100 Å to about 500 Å.

15. The method of claim 12 wherein the first material includes n-type impurities, and wherein the second material includes p-type impurities.

16. The method of claim 12 wherein the removing a portion of the gate material includes:

removing a portion of the gate material to isolate gate material on one side of the insulating layer from gate material on an opposite side of the insulating layer.

17. The method of claim 16 wherein a width of the removed portion ranges from about 100 Å to about 500 Å.

18. A method for forming a semiconductor device from a device that includes a first source region, a first drain region, and a first fin structure that are separated from a second source region, a second drain region, and a second fin structure by an insulating layer, the method comprising:

forming a dielectric layer over the device;

removing portions of the dielectric layer to create covered portions and bare portions;

depositing a gate material over the covered portions and bare portions;

doping the first fin structure, the first source region, and the first drain region with a first material;

doping the second fin structure, the second source region, and the second drain region with a second material; and

removing a portion of the gate material over at least one covered portion to form the

semiconductor device.

19. The method of claim 18 wherein the removing a portion of the gate material includes:

removing the portion of gate material positioned above the insulating layer.

20. The method of claim 18 wherein the first material includes n-type impurities, and wherein the second material includes p-type impurities.